Amended claims:

B '	1. (Amended) A device formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the device comprising: a well of a second conductivity type formed in the semiconductor material, the well having a dopant concentration; a first region of the second conductivity type formed in the well, the first region having a dopant concentration greater than the dopant concentration of the well, the first region being connected to a first node; a second region of the first conductivity type formed in the well, the second region having a dopant concentration greater than the dopant concentration of the semiconductor material, the second region being connected to the first node; a third region of the second conductivity type formed in the semiconductor material, the third region having a dopant concentration greater than the dopant concentration of the well, the third region being connected to a second node, and
	a fourth region of the first conductivity type formed in the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, the fourth region being connected to the second node, wherein the second region is reduced in size compared to a conventional LVTSCR of the same process. 3. (Amended) The device of claim 2, wherein the third region is increased in size relative to
62	that of a conventional LVTSCR of the same process, to reduce space charge
	neutralization.
ც	9. (Amended) A method of providing a device having a higher holding voltage than a LVTSCR and supporting a higher current than a GGNMOS, comprising providing a LVTSCR-like structure having a p+ emitter that is sufficiently reduced in size so as to increase the holding voltage to a desired level.
BA	11. A method of creating an ESD protection structure having a higher holding voltage than a conventional LVTSCR, comprising providing a LVTSCR-like structure, and manipulating the size of the p+ emitter. 12. A method of claim 11, further comprising using TCAD simulations to determine a p+ emitter size corresponding to a desired holding voltage. 13. A method of creating an ESD protection structure that supports a higher current than a conventional GGNMOS device, comprising providing a LVTSCR-like structure, and manipulating the size of the p+ emitter. 14. A method of claim 13, further comprising using TCAD simulations to determine a p+ emitter size corresponding to a desired current. 15. A method of varying the holding voltage of a LVTSCR, comprising adjusting the size of the p+ emitter.

	16.	A method of claim-15, further comprising adjusting the size of the n+ emitter.
B ⁴ contal	17.	A method of adjusting the holding voltage of an ESD protection structure that includes a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration; a well of a second conductivity type formed in the semiconductor material, the well having a dopant concentration; a first region of the second conductivity type formed in the well, the first region having a dopant concentration greater than the dopant concentration of the well, the first region being connected to a first node; a second region of the first conductivity type formed in the well, the second region having a dopant concentration greater than the dopant concentration of the semiconductor material, the second region being connected to the first node; a third region of the second conductivity type formed in the semiconductor material, the third region having a dopant concentration greater than the dopant concentration of the well, the third region being connected to a second node, and a fourth region of the first conductivity type formed in the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, the fourth region being connected to the second node, comprising, adjusting the size of the second region. A method of claim 17, further comprising adjusting the size of the third region.